



AOD403

P-Channel Enhancement Mode Field Effect Transistor

General Description

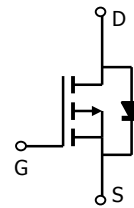
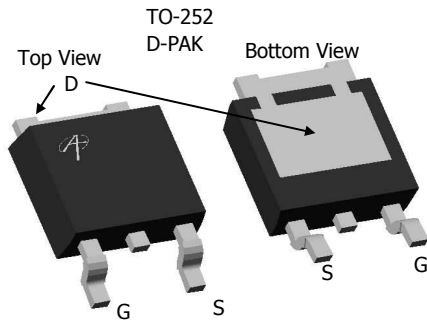
The AOD403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free*

Features

- V_{DS} (V) = -30V
- I_D = -85A (V_{GS} = -20V)
- $R_{DS(ON)} < 6m\Omega$ (V_{GS} = -20V)
- $R_{DS(ON)} < 7.6m\Omega$ (V_{GS} = -10V)

UIS TESTED!
Rg,Ciss,Coss,Crss Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^{B,G}	I_D	$T_A=25^\circ\text{C}^G$	A
		$T_A=100^\circ\text{C}^B$	
Pulsed Drain Current	I_{DM}	-200	
Avalanche Current ^C	I_{AR}	-30	A
Repetitive avalanche energy $L=0.1\text{mH}^C$	E_{AR}	120	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	13	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	39	50
Maximum Junction-to-Case ^C	$R_{\theta JC}$	0.56	1.5	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		-0.01	-1	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 25\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.5	-2.6	-3.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-20\text{V}$, $I_D=-20\text{A}$ $T_J=125^\circ\text{C}$		5.1	6	$\text{m}\Omega$
		$V_{GS}=-10\text{V}$, $I_D=-20\text{A}$		7.1	8.5	$\text{m}\Omega$
		$V_{GS}=-10\text{V}$, $I_D=-20\text{A}$		6.3	7.6	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-20\text{A}$		44		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.72	-1	V
I_S	Maximum Body-Diode Continuous Current ^G				-80	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		4360	5300	pF
C_{oss}	Output Capacitance			1050		pF
C_{rss}	Reverse Transfer Capacitance			762		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.5	3	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-20\text{A}$		93.2	120	nC
Q_{gs}	Gate Source Charge			18		nC
Q_{gd}	Gate Drain Charge			29.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$		18	25	ns
t_r	Turn-On Rise Time			30	45	ns
$t_{D(off)}$	Turn-Off DelayTime			51	75	ns
t_f	Turn-Off Fall Time			35	50	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		39.5	48	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		30.8	37	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB or heatsink allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300 \mu\text{s}$ pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by the package current capability.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev 6: Sep 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

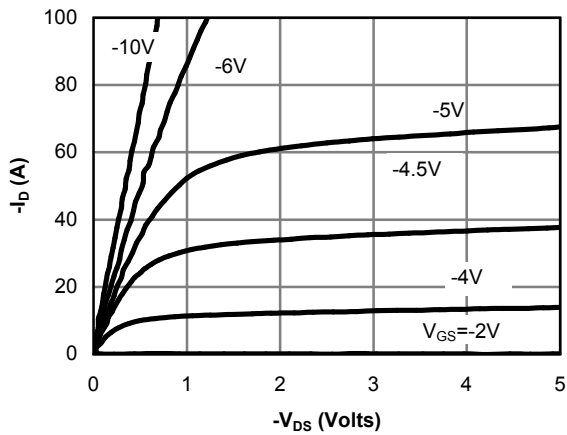


Fig 1: On-Region Characteristics

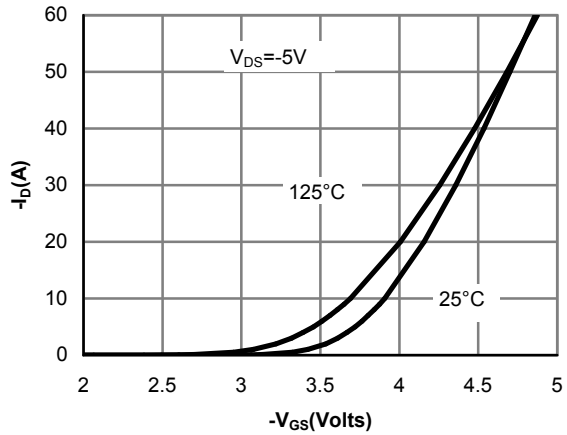


Figure 2: Transfer Characteristics

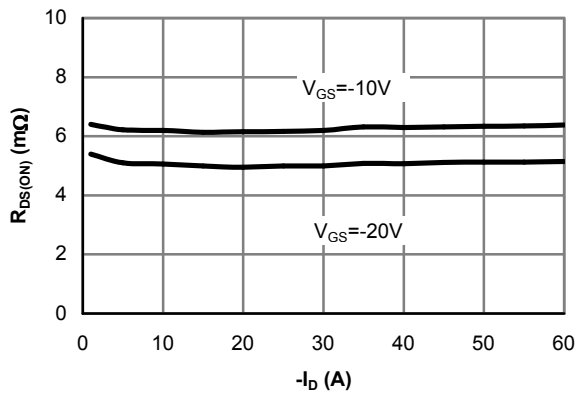


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

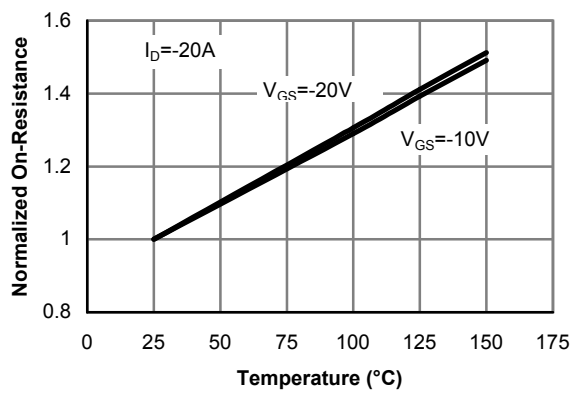


Figure 4: On-Resistance vs. Junction Temperature

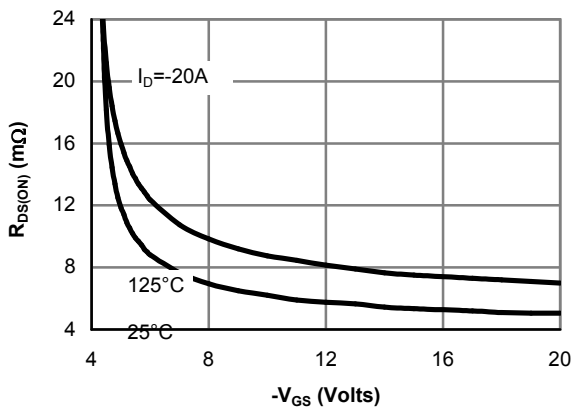


Figure 5: On-Resistance vs. Gate-Source Voltage

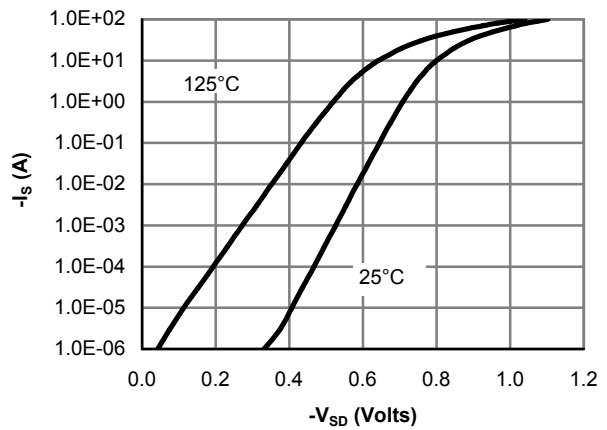


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

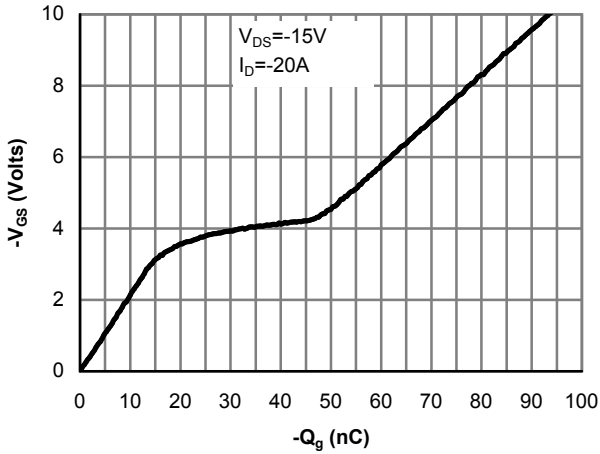


Figure 7: Gate-Charge Characteristics

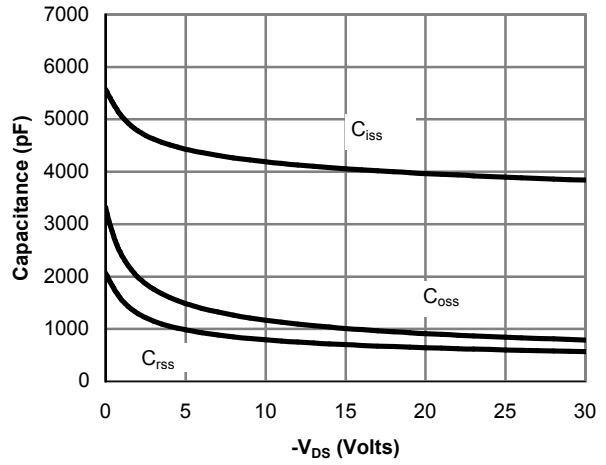


Figure 8: Capacitance Characteristics

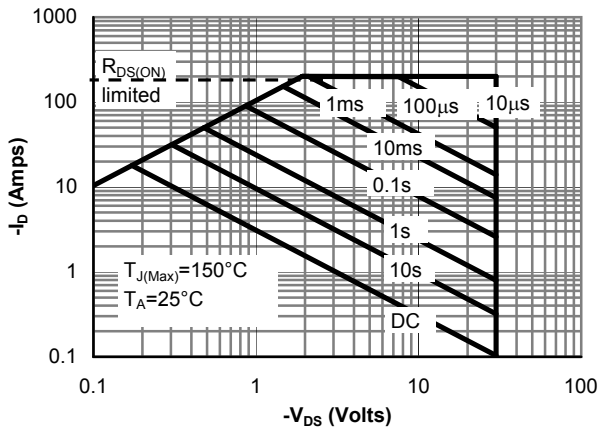


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

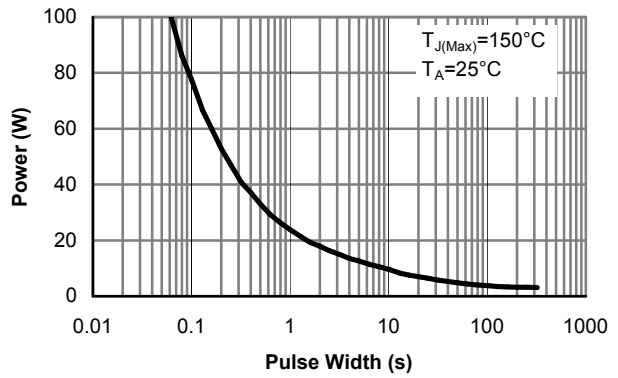


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

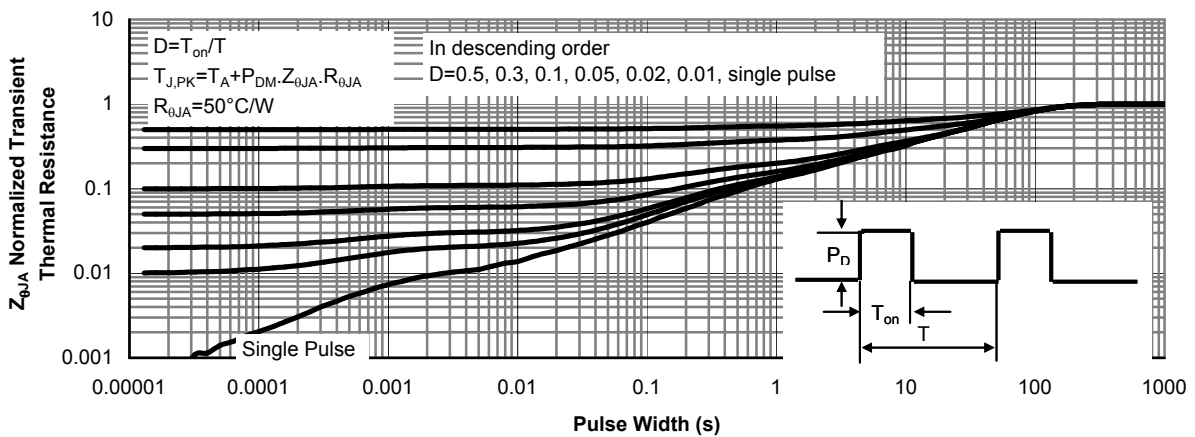
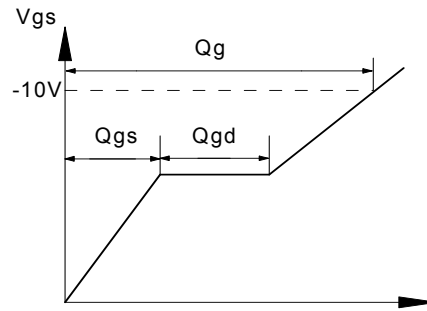
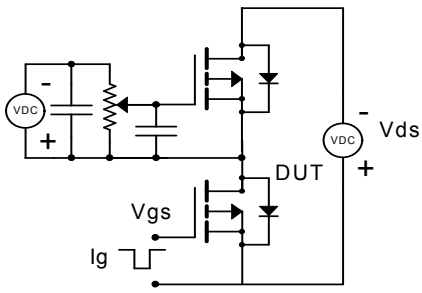
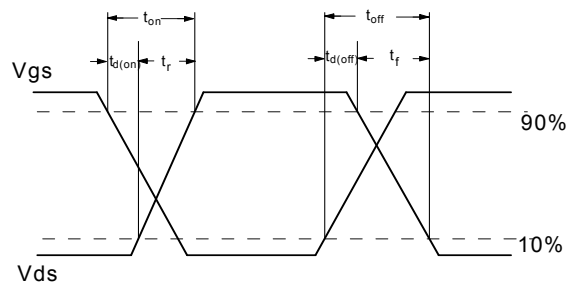
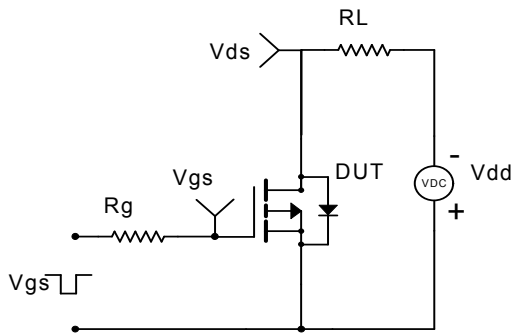


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

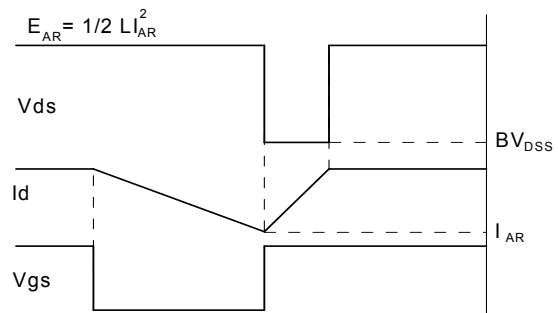
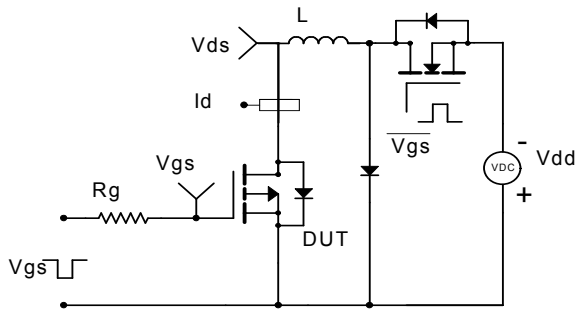
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

